

## [CLAIMS]

A  
A  
A  
Sub  
C  
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3  
1. A bus, having at least an address remapper ~~(1)~~ defining two sections ~~(3, 4)~~ in the bus, each section comprising at least one station ~~(5-9)~~ having a physical address, wherein a station on one section of the bus is assigned a dummy address for being addressed by a station on the other section, the address remapper remapping a dummy address from the other section into a physical address to the ~~one section.~~

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2. A bus according to claim 1, wherein the format of a physical address comprises a fixed part and a setable part, and wherein the dummy address is obtained by changing at least one bit of the fixed part of the physical address.

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3. A bus according to claim 1 ~~or 2~~, wherein the dummy addresses for stations out of a given section are different from the physical addresses for stations in said given section.

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4. An address remapper for a bus, comprising  
 - terminals ~~(21-24)~~ for connecting two sections of the bus;  
 - address detecting means ~~(30)~~ for detecting an address received from one section of the bus;  
 - address remapping means ~~(32, 26, 34)~~ for remapping the address and transmitting the remapped address to the other section of the bus.

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5. An address remapper according to claim 4, wherein the bus is a two wire serial bus, and wherein the address detecting means ~~(30)~~ detect a transition of the value on one wire while the other wire is a given level.

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6. An address remapper according to claim 4 ~~or 5~~, wherein the bus is a two wire serial bus, and wherein the address remapping means comprise means ~~(34)~~ for bringing one wire to a given level.

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7. An address remapper according to claim 4, ~~5 or 6~~, wherein the bus is a two wire serial bus having one data wire and one clock wire,

A the terminals ~~(23, 24)~~ for the clock wire of each section being connected.

5 ~~Site 81~~ 8. An address remapper according to claim 7, wherein the address remapping means comprise switching means for selectively connecting the terminals ~~(21, 22)~~ for the data wire of each section.

10. A process for connecting two sections of a bus, by transmitting data from one section of the bus to the other section of the bus,

10 comprising the steps of

- detecting an address sent from one section of the bus to the other section of the bus;
- remapping the address before transmitting it to the other section of the bus.

15 11. A process according to claim 10, wherein the step of detecting comprises detecting a START condition preceding an address.

20 12. A process according to claim 11, wherein the step of remapping comprises changing at least one bit of an address, preferably one bit of a fixed part of an address.

Add A1

Add C2

Add 11